Dillan Mills

Senior Computer Engineer

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About me

Computer engineer who employs problem solving and strategic thinking to find solutions. Highly motived in seeking opportunities for growth. Dedicated and passionate about computer science and electrical engineering. Currently utilizing both fields of study as a microchip verification engineer at Synopsys, Inc.

Skills

Verilog/SystemVerilog

UVM Verification

VHDL

Python

Perl
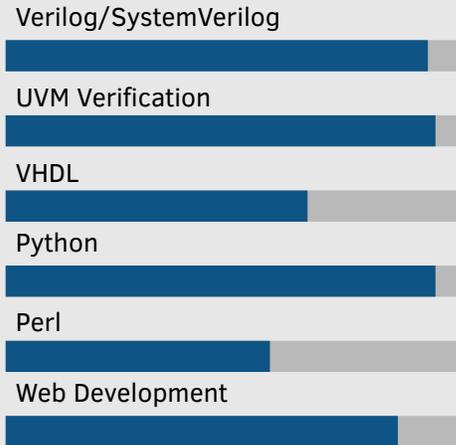
Web Development

FPGA⋆5 JavaScript⋆6 Java⋆3
MATLAB⋆3 C/C++⋆4 HTML⋆6

(*)[The skill scale is from 0 (Fundamental Awareness) to 6 (Expert).]

Interests

Pushing the boundaries of software in the hardware development industry, with some web development on the side.

Education

2015–2018	B.Sc. magna cum laude	Northern Arizona University
	Majoring in Electrical Engineering, Computer Engineering Emphasis	
	B.Sc. magna cum laude	
	Majoring in Computer Science	
	GPA: 3.9	

Experience

since 2021	Senior Verification Engineer	FirstPass Engineering (A Synopsys Company)

- Drive stimulus generation and coverage closure for a highly complex memory interface design
- Leverage Object-Oriented programming skills to rework and improve the stimulus generation components of the testbench, allowing for better scaling of stimulus, quicker test creation, and easier failure debugging
- Develop and use novel UVM testbench architecture techniques including policy-based stimulus randomization and randsequence

2016–2021	Verification Engineer	Microchip Technology

- Develop IP block level test plans, UVM testbenches, constrained random test sequences and continuous assertions to close 100% functional and code coverage on each IP
- Integration of IP blocks into chip level SoC system blocks, perform gate level simulation checking and close 100% coverage on each SoC
- Lead developer of the team software Python and Perl scripts, including new feature development and user support, handling bug reports and implementing patches as needed

2016–2018	Student Researcher	NAU Independent Research

- Worked individually to create a custom softcore processor in SystemVerilog based off the design specs for the TI MSP430 processor
- Worked with the Air Force Research Laboratory, successfully expanded the custom MSP430 to support ternary instructions and data
- Used the custom MSP430 as the basis for a capstone project while implementing a hardware-based publish/subscribe coprocessor for Internet of Things devices to improve design and simplify programming

Publications

DVCon 20	SystemVerilog Configurations and Tool Flow Using SCons (An Improved Make)
DVCon 21	How to Overcome Editor Envy: Why Can't My Editor Do That?

Trainings and Certifications

Sutherland HDL

- Verilog/System Verilog for Design and Synthesis
- System Verilog Object Oriented Verification
- Mastering System Verilog UVM
- System Verilog Assertions for Design Engineers and Verification Engineers